14. The semiconductor device of claim 10, wherein said trench is disposed above a gate structure.

15. The semiconductor device of claim 10, wherein said trench is disposed adjacent to a source structure.

16. The semiconductor device of claim 10, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness.

17. The semiconductor device of claim 10, wherein said silicon dioxide layer is thermally grown.

18. The semiconductor device of claim 10, wherein said silicon dioxide layer is deposited.

19. The electronic silicon device of claim 1, wherein the polysilicon fill disposed on the second portion of said wall is in contact with a doped region of said silicon substrate.

20. The semiconductor device of claim 10, wherein the polysilicon fill disposed on the second portion of said wall is in contact with a doped region of said silicon substrate.

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